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L4: Entry 1 of 8 File: PGPB Oct 23, 2003

DOCUMENT-IDENTIFIER: US 20030200473 A1
TITLE: System and method for activity or event based dynamic energy conserving server reconfiguration

Detail Description Paragraph (20):
[0055] Furthermore, in one embodiment, every node in a cluster of nodes is identical as they come from the factory, and any node may be adapted, such as through software that is loaded into a node, to provide any one of a plurality of available functions. In another embodiment, somewhat to very different node structures are provided within a single cluster to provide more highly optimized network nodes, computer nodes, and monitor nodes. The existence and distribution of such nodes in a cluster may be selected by the customer or user so that each cluster provides the desired number of computer, monitor, network, or other nodes as may become available. Advantageously, the nodes are implemented as plug-in or removable modules, such as printed circuit boards, so that the configuration of any particular cluster or of a system having a plurality of clusters may be modified after manufacture. In this way additional nodes of any desired type may be added when the need arises. Not all locations within a cluster need be populated thereby providing initial cost savings as well as allowing later expansion. Nodes may be dynamic configured, either identical nodes or specialized nodes, are supported in response to changing loading and QOS.

Detail Description Paragraph (30):
[0065] In another aspect, the inventive structure and method may be transformed, morphed, or otherwise configured to provide (either alone or in combination with other cluster units) a great variety of organizations and architectural topologies, and therefore provide an almost unlimited number of functional configurations. In another aspect, all nodes within an enclosure are connected to each other and to a switching means by a backplane bus internal to the enclosure, thereby eliminating the need for external node-to-node and node-to-switch connection cables. Such conventional cables are prone to failure and inadvertent disconnection during service operations that may result in network downtime. In yet another aspect, the inventive structure and method facilitates and permits any node to perform any supported function or operation. In one embodiment, all nodes are identical and can be adapted, such as by programming or loading appropriate software, to provide any function or operation. In another embodiment, different classes or types of nodes are provided that are somewhat specialized and/or optimized to perform selected classes of functions or operations very well. In yet another embodiment, highly specialized nodes are available to perform specific functions. In each of these embodiments, the nodes are desirably provided as removable hot-pluggable modular units, such as PC boards or cards, that may be added or removed from the enclosure without powering off or otherwise making the network unavailable. This facilitates the interchange of hot spares which may remain ready and available within the enclosure for immediate use in the event of a node failure. In still another aspect, each Integrated Server System (or cluster) unit is cascadable so that multiple sets of nodes may be interconnected to provide the desired number and type of operation. In yet another aspect, any and all nodes are reconfigurable at any time based on such factors as load or quality of service (QOS) requirements.

Furthermore, the change or reconfiguration may be communicated to other nodes and the effect of such reconfiguration ripple through to the other nodes and to the network as a whole. This permits the entire system to be self balancing to the extent desired. In another aspect, each cluster is provided with sufficient intelligence so that at least some network administration operations that conventionally required some degree of supervision or intervention may be performed autonomously and dynamically in response to sensed conditions experienced on the network or within one or more nodes of the network.

Detail Description Paragraph (68):
[0103] From a somewhat different perspective, variations in server architecture, reflect the variations in personal computers, mainframes, and computing systems generally. The vast structural, architectural, methodological, and procedural variations inherent in computer systems having chips, chipsets, and motherboards adapted for use by Intel Processors (such as the Intel x86, Intel Pentium.TM., Intel Pentium.TM. II, Intel Pentium.TM. III, Intel Pentium.TM. IV), Transmeta Crusoe.TM. with LongRun.TM., AMD, Motorola, and others, precludes a detailed description of the manner in which the inventive structure and method will be applied in each situation. Therefore in the sections that follow, aspects of the inventive power management and ISS system architecture are described first in a general case to the extent possible, and second relative to a particular processor/system configuration (the Transmeta Crusoe Processor). Those having ordinary skill will appreciate in light of the description that the inventive structure and method apply to a broad set of different processor and computer/server architecture types and that minor variations within the ordinary skill of a practitioner in the field may be made to adapt the invention to other processor/system environments.

Detail Description Paragraph (201):
[0236] In FIG. 19, the Mode 1 to Mode 2 AA' transitions are locally controlled. For example, in the Intel SpeedStep.TM. CPUs the AA' transitions are controlled using control mechanisms provided by Intel on their CPU chips that permit a system designer to issue a command to the CPU to transition it from Mode 1 to Mode 2 under an identified condition and from Mode 2 to Mode 1 under a second identified condition. Similarly, the Transmeta Crusoe CPUs implementing their LongRun technology would transition from Mode 1 to a selected one of a plurality of Mode 2 states, and from that Mode 2 state (or a different Mode 2 state) to Mode 1, under identified conditions. These conditions are known in the art, available from Intel or Transmeta, or from Intel, AMD, or Transmeta computer manufacturer OEMs, and not described here in greater detail

L2: Entry 1 of 1 File: USPT Jan 31, 1984

DOCUMENT-IDENTIFIER: US 4428269 A
TITLE: Chord teaching system and method for an electronic musical instrument

Detailed Description Text (3):
The chord teaching system operates in seven different modes namely, one finger chords, three finger chords, chord quiz, program, program plus one finger chords, program plus three finger chords, and program plus autoperform. A mode control panel comprising a plurality of switches is located on the console of the organ and the organist selects the mode of operation by actuating these switches. In one mode of operation of the chord teaching system a rhythm unit under control of the organ's rhythm clock controls the timing at which pre-selected chords are played and the keys forming the playing chord are indicated to the learning organist. A chord type selector comprising a plurality of switches is also located on the console of the organ and the organist selects the type of chord to be learned and/or played by the chord teaching system by actuating these switches. The types of chordes that can be selected by the learning organist are major, minor, seventh, minor seventh, major seventh, diminished, sixth or augmented.

Detailed Description Text (72):
In the preferred embodiment, the first chord sounds at the first beat of the measure since the rhythm unit begins at beat 1 of a typical measure. Of course, it will be obvious to those of ordinary skill that the chord could be sounded at other times under control of the rhythm unit. If the rhythm unit is running in 4/4 time the first stored chord is sounded at the first beat and the second stored chord is sounded at the third beat of the measure while if the rhythm unit is running in 3/4 time the first chord is sounded at the first beat of the first measure and the second chord is sounded at the first beat of the second measure. The chord playback is controlled by the rhythm unit of the organ. This operation of the system must be followed during the programming function described in FIG. 4d so that if the song to be played is in 4/4 time amd if a whole note is needed then the chord is entered twice since the 4/4 time causes the stored chords to be sounded at the first and third beat of a measure and the double entry results in the sound of a whole note as opposed to two half notes. However, no timing information is stored during the programming the chord and the playback is under the control of the rhythm unit.

L4: Entry 1 of 8 File: PGPB Oct 23, 2003

DOCUMENT-IDENTIFIER: US 20030200473 A1
TITLE: System and method for activity or event based dynamic energy conserving server reconfiguration

Detail Description Paragraph (20):
[0055] Furthermore, in one embodiment, every node in a cluster of nodes is identical as they come from the factory, and any node may be adapted, such as through software that is loaded into a node, to provide any one of a plurality of available functions. In another embodiment, somewhat to very different node structures are provided within a single cluster to provide more highly optimized network nodes, computer nodes, and monitor nodes. The existence and distribution of such nodes in a cluster may be selected by the customer or user so that each cluster provides the desired number of computer, monitor, network, or other nodes as may become available. Advantageously, the nodes are implemented as plug-in or removable modules, such as printed circuit boards, so that the configuration of any particular cluster or of a system having a plurality of clusters may be modified after manufacture. In this way additional nodes of any desired type may be added when the need arises. Not all locations within a cluster need be populated thereby providing initial cost savings as well as allowing later expansion. Nodes may be dynamic configured, either identical nodes or specialized nodes, are supported in response to changing loading and QOS.

Detail Description Paragraph (30):
[0065] In another aspect, the inventive structure and method may be transformed, morphed, or otherwise configured to provide (either alone or in combination with other cluster units) a great variety of organizations and architectural topologies, and therefore provide an almost unlimited number of functional configurations. In another aspect, all nodes within an enclosure are connected to each other and to a switching means by a backplane bus internal to the enclosure, thereby eliminating the need for external node-to-node and node-to-switch connection cables. Such conventional cables are prone to failure and inadvertent disconnection during service operations that may result in network downtime. In yet another aspect, the inventive structure and method facilitates and permits any node to perform any supported function or operation. In one embodiment, all nodes are identical and can be adapted, such as by programming or loading appropriate software, to provide any function or operation. In another embodiment, different classes or types of nodes are provided that are somewhat specialized and/or optimized to perform selected classes of functions or operations very well. In yet another embodiment, highly specialized nodes are available to perform specific functions. In each of these embodiments, the nodes are desirably provided as removable hot-pluggable modular units, such as PC boards or cards, that may be added or removed from the enclosure without powering off or otherwise making the network unavailable. This facilitates the interchange of hot spares which may remain ready and available within the enclosure for immediate use in the event of a node failure. In still another aspect, each Integrated Server System (or cluster) unit is cascadable so that multiple sets of nodes may be interconnected to provide the desired number and type of operation. In yet another aspect, any and all nodes are reconfigurable at any time based on such factors as load or quality of service (QOS) requirements.

Furthermore, the change or reconfiguration may be communicated to other nodes and the effect of such reconfiguration ripple through to the other nodes and to the network as a whole. This permits the entire system to be self balancing to the extent desired. In another aspect, each cluster is provided with sufficient intelligence so that at least some network administration operations that conventionally required some degree of supervision or intervention may be performed autonomously and dynamically in response to sensed conditions experienced on the network or within one or more nodes of the network.

Detail Description Paragraph (68):
[0103] From a somewhat different perspective, variations in server architecture, reflect the variations in personal computers, mainframes, and computing systems generally. The vast structural, architectural, methodological, and procedural variations inherent in computer systems having chips, chipsets, and motherboards adapted for use by Intel Processors (such as the Intel x86, Intel Pentium.TM., Intel Pentium.TM. II, Intel Pentium.TM. III, Intel Pentium.TM. IV), Transmeta Crusoe.TM. with LongRun.TM., AMD, Motorola, and others, precludes a detailed description of the manner in which the inventive structure and method will be applied in each situation. Therefore in the sections that follow, aspects of the inventive power management and ISS system architecture are described first in a general case to the extent possible, and second relative to a particular processor/system configuration (the Transmeta Crusoe Processor). Those having ordinary skill will appreciate in light of the description that the inventive structure and method apply to a broad set of different processor and computer/server architecture types and that minor variations within the ordinary skill of a practitioner in the field may be made to adapt the invention to other processor/system environments.

Detail Description Paragraph (201):
[0236] In FIG. 19, the Mode 1 to Mode 2 AA' transitions are locally controlled. For example, in the Intel SpeedStep.TM. CPUs the AA' transitions are controlled using control mechanisms provided by Intel on their CPU chips that permit a system designer to issue a command to the CPU to transition it from Mode 1 to Mode 2 under an identified condition and from Mode 2 to Mode 1 under a second identified condition. Similarly, the Transmeta Crusoe CPUs implementing their LongRun technology would transition from Mode 1 to a selected one of a plurality of Mode 2 states, and from that Mode 2 state (or a different Mode 2 state) to Mode 1, under identified conditions. These conditions are known in the art, available from Intel or Transmeta, or from Intel, AMD, or Transmeta computer manufacturer OEMs, and not described here in greater detail

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L4: Entry 8 of 8 File: PGPB Jan 10, 2002

DOCUMENT-IDENTIFIER: US 20020004912 A1
TITLE: System, architecture, and method for logical server and other network devices in a dynamically configurable multi-server network environment

Detail Description Paragraph (20):
[0055] Furthermore, in one embodiment, every node in a cluster of nodes is identical as they come from the factory, and any node may be adapted, such as through software that is loaded into a node, to provide any one of a plurality of available functions. In another embodiment, somewhat to very different node structures are provided within a single cluster to provide more highly optimized network nodes, computer nodes, and monitor nodes. The existence and distribution of such nodes in a cluster may be selected by the customer or user so that each cluster provides the desired number of computer, monitor, network, or other nodes as may become available. Advantageously, the nodes are implemented as plug-in or removable modules, such as printed circuit boards, so that the configuration of any particular cluster or of a system having a plurality of clusters may be modified after manufacture. In this way additional nodes of any desired type may be added when the need arises. Not all locations within a cluster need be populated thereby providing initial cost savings as well as allowing later expansion. Nodes may be dynamic configured, either identical nodes or specialized nodes, are supported in response to changing loading and QOS.

Detail Description Paragraph (30):
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reconfigurable at any time based on such factors as load or quality of service (QOS) requirements. Furthermore, the change or reconfiguration may be communicated to other nodes and the effect of such reconfiguration ripple through to the other nodes and to the network as a whole. This permits the entire system to be self balancing to the extent desired. In another aspect, each cluster is provided with sufficient intelligence so that at least some network administration operations that conventionally required some degree of supervision or intervention may be performed autonomously and dynamically in response to sensed conditions experienced on the network or within one or more nodes of the network.

Detail Description Paragraph (68):
[0103] From a somewhat different perspective, variations in server architecture, reflect the variations in personal computers, mainframes, and computing systems generally. The vast structural, architectural, methodological, and procedural variations inherent in computer systems having chips, chipsets, and motherboards adapted for use by Intel Processors (such as the Intel x86, Intel Pentium.TM., Intel Pentium.TM. II, Intel Pentium.TM. III, Intel Pentium.TM. IV), Transmeta Crusoe.TM. with LongRun.TM., AMD, Motorola, and others, precludes a detailed description of the manner in which the inventive structure and method will be applied in each situation. Therefore in the sections that follow, aspects of the inventive power management and ISS system architecture are described first in a general case to the extent possible, and second relative to a particular processor/system configuration (the Transmeta Crusoe Processor). Those having ordinary skill will appreciate in light of the description that the inventive structure and method apply to a broad set of different processor and computer/server architecture types and that minor variations within the ordinary skill of a practitioner in the field may be made to adapt the invention to other processor/system environments.

Detail Description Paragraph (201):
[0236] In FIG. 19, the Mode 1 to Mode 2 ADA' transitions are locally controlled. For example, in the Intel SpeedStep.TM. CPUs the A*A' transitions are controlled using control mechanisms provided by Intel on their CPU chips that permit a system designer to issue a command to the CPU to transition it from Mode 1 to Mode 2 under an identified condition and from Mode 2 to Mode 1 under a second identified condition. Similarly, the Transmeta Crusoe CPUs implementing their LongRun technology would transition from Mode 1 to a selected one of a plurality of Mode 2 states, and from that Mode 2 state (or a different Mode 2 state) to Mode 1, under identified conditions. These conditions are known in the art, available from Intel or Transmeta, or from Intel, AMD, or Transmeta computer manufacturer OEMs, and not described here in greater detail

L7: Entry 12 of 27 File: USPT Sep 4, 2001

DOCUMENT-IDENTIFIER: US 6286111 B1
TITLE: Retry mechanism for remote operation failure in distributed computing environment

Abstract Text (1):
The present invention provides a mechanism for retrying a system operation on a remote node in a distributed environment. In an "optimistic" embodiment of the invention, a local system issues a set of commands over a network to a remote node to perform a system operation. Responsive to a failure by the remote node to perform the requested system action, the retry mechanism determines whether the remote node could be in a nonoperational state. If the remote node could be in the nonoperational state, the system issues a magic packet to the remote node. Next, the system waits a predetermined period of time for the remote node to be brought to a fully operational state. The system issues the set of commands a second time to the remote node to perform the system operation. In a "preemptive" or "pessimistic" embodiment of the invention, the likelihood that the remote node is in a powered down or similar state is sufficiently high to outweigh the cost of sending a magic packet over the network. Thus, to perform a system operation on a remote node, a magic packet is issued preemptively to the remote node over a network to bring it to a fully operational state. Then, the local system issues a set of commands over the network to the remote node to perform the system operation.

Brief Summary Text (8):
The present invention provides a mechanism for retrying a system operation on a remote node in a distributed environment. In an "optimistic" embodiment of the invention, a local system issues a set of commands over a network to a remote node to perform a system operation. Responsive to a failure by the remote node to perform the requested system action, the retry mechanism determines whether the remote node could be in a "node-down" or similar nonoperational state. If the remote node could be in the "node-down" state, the system issues a magic packet to the remote node. Next, the system waits a predetermined period of time for the remote node to be brought to a fully operational state. The system issues the set of commands a second time to the remote node to perform the system operation. In a "preemptive" or "pessimistic" embodiment of the invention, the likelihood that the remote node is in a "node-down" or similar state is sufficiently high to outweigh the cost of sending a magic packet over the network. Thus, expecting failure of a request for a system operation on a remote node, a magic packet is issued preemptively to the remote node over a network to bring it to a fully operational state. Then, the local system issues a set of commands over the network to the remote node to perform the system operation.

Detailed Description Text (8):
Referring now to FIG. 2, the invention is preferably implemented in a large distributed computer environment 100 comprising up to thousands or even tens of thousands of "nodes." At each node, will be located a system generally similar to that described above. The nodes will typically be geographically dispersed and the overall environment is "managed" in a distributed manner. Preferably, the managed environment (ME) is logically broken down into a series of loosely-connected managed regions (MR)

112, each with its own server 114 for managing local resources with the MR. Multiple servers 114 coordinate activities across the enterprise and permit remote site management and operation. Each server 114 serves a number of gateway machines 116, each of which in turn support a plurality of endpoints 118. The server 114 coordinates all activity within the MR using a terminal node manager 120.

Detailed Description Text (18):
Furthermore, although the preferred embodiment uses the Magic Packet technology developed by the AMD Corporation and licensed by many personal computer manufacturers, other similar mechanisms are encompassed by the invention. That is, any specific message which is recognized by nodes in the distributed environment as a command to "wake up" and bring themselves to an operational state should be considered a "magic packet" whether or not it exactly conforms to the details of the Magic Packet technology described below.

Detailed Description Text (41):
Hewlett-Packard, IBM, Gateway and other leading manufacturers implement AMD's Magic Packet technology.

DOCUMENT-IDENTIFIER: US 6157244 A
TITLE: Power supply independent temperature sensor

Detailed Description Text (5):
The band gap reference circuit 102 includes a plurality of transistors that have gate terminals connected to a PGATE line. Specifically, the bandgap reference circuit 102 includes three P-channel MOS transistors P23, P24 and P31, two N-channel MOS transistors N25 and N26, two resistors TCRES1 and TCRES2, and three diode-connected PNP bipolar transistors Q8, Q7<0:8> and Q9<0:8>. The gates of P-channel MOS field effect transistors P23, P24, and P31 in the bandgap reference circuit 102 and P-channel MOS field effect transistor P32 in the biasing circuit 110 are connected to the drain of P-channel MOS field effect transistor P24 so that the P-channel MOS field effect transistors P23, P24, P31 and P32 form a current mirror where P-channel MOS field effect transistors P23, P31 and P32 mirror the second current through P-channel MOS field effect transistor P24. The V.sub.BE node and the IPTAT node are driven to identical voltages by N-channel MOS field effect transistors N25 and N26, which are laid out identically, have the same size, and have the same gate connections. The resistor TCRES1 is positioned between the IPTAT node and the PNP bipolar transistor Q7<0:7> so that the voltage drop across the resistor TCRES1 corresponds to the difference in base-emitter voltages .DELTA.V.sub.BE of the PNP bipolar transistors Q8 and Q7<0:7>.

Detailed Description Text (22):
The first current I.sub.1 and the second current I.sub.2 are essentially identical so that PNP bipolar transistor Q7<0:8> is eight times the size of PNP bipolar transistor Q8 and the current density in PNP bipolar transistor Q8 is eight times the current density in PNP bipolar transistor Q7<0:8>. The temperature coefficient of a base-emitter voltage drop increases to a greater absolute magnitude as the current density decreases. As temperature increases, the base-emitter voltage V.sub.BE-Q7<0:8> of PNP bipolar transistor Q7<0:8> decreases more rapidly than the base-emitter voltage V.sub.BE-Q8 of transistor Q8. However, the voltages at V.sub.BE node and IPTAT node are essentially mutually identical. The base-emitter voltage of PNP bipolar transistor Q8 is essentially identical to the voltage drop across resistor TCRES1 plus the base-emitter voltage of PNP bipolar transistors Q7<0:8>. Since the difference between the base-emitter voltages of PNP bipolar transistors Q8 and Q7<0:8> increases as temperature increases, the voltage drop across resistor TCRES1 also increases as temperature increases. The voltage drop across resistor TCRES1 increases as temperature increases not only because the second current increases as temperature increases, but also because resistor TCRES1 has a positive temperature coefficient.

Detailed Description Text (43):
Referring to FIG. 12, a schematic block diagram illustrates an embodiment of an AMD-K6 microprocessor 500. The microprocessor 500 is an X86 instruction set-compatible microprocessor implementing a set of Multi-Media eXtenstions (MMX). A level-one (L1) instruction cache 502 begins predecoding instructions obtained from a processor system bus interface 504 during filling of the 32KB

two-way associative L1 instruction cache 502. The L1 instruction cache 502 includes a 64-entry instruction translational lookahead buffer (ITLB) 546. Bypass (not shown) and storage buffers (not shown) for instructions (4.times.16) and predecode (4.times.20) to the L1 instruction cache 502 are supplied to allow data-in and data flow-back to cache output terminals.

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L7: Entry 27 of 27 File: USPT Oct 14, 1986

DOCUMENT-IDENTIFIER: US 4617473 A
TITLE: CMOS backup power switching circuit

Detailed Description Text (14):
The potential appearing at node 106 is coupled from the first stage 66 to the second stage 68 whereat it is connected to the control input 108 of a fifth p-channel MOS transistor 110. The input 118 of transistor 110 is coupled to the output 42 of the power transistor 40. The output 124 of transistor 110 is coupled to a node 52 (identical to the output 52 of the differential comparator 36) which is in turn coupled to the input 126 of a fourth n-channel MOS transistor 116, whose output 120 is coupled to the reference input 28. The control input 122 of transistor 116 is coupled to the control input 90 of transistor 92 located in the first stage 66.

Detailed Description Text (16):
The input 136 of transistor 130 is coupled to the output 42 of the power transistor 40. The output 144 of transistor 130 is coupled to a node 58 (identical to the ouput of 58 of the inverter 56) which is in turn coupled to the input 146 of transistor 132. The output 138 of transistor 132 is coupled to the reference input 28.

Detailed Description Text (18):
The first stage 66 of the differential comparator 36 is comprised of the n-channel MOS differential pair, transistors 72 and 76, fed by a current mirror p-channel MOS transistor pair, transistors 98 and 104. A bias for the first stage 66 is provided by the resistor 86 and the transistor 92. The second stage 68, comprising transistors 110 and 116, provides additional voltage gain through the differential comparitor 36. The transistors 92 amd 116 may be considered to be a second current source through the first stage 66 and the second stage 68, respectively.